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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,925	05/04/2005	Makoto Shimizu	10921.320USWO	4573

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EXAMINER	
HSU, AMY R	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
11/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,925	SHIMIZU, MAKOTO	
	Examiner	Art Unit	
	Amy Hsu	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3-14 and 19-23* is/are allowed.

6)☒ Claim(s) *2,15 and 16* is/are rejected.

7)☒ Claim(s) *17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/6/2006, 5/4/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Izawa et al. (JP 06-098080).

Regarding Claim 2, Izawa teaches an area image sensor (*"solid state image sensor" in paragraph 4)* comprising a plurality of pixels arranged in a lattice shape on an imaging face for photoelectrically converting light of a subject optical image that is focused on the imaging face via an imaging optical system into an electrical signal in each pixel and outputting the electrical signal, each pixel comprising (*Drawing 1, shows a "pixel cell" see paragraph 7)*: a photoelectric conversion element that converts light rendered through exposure by accumulating electrical charge in accordance with a received light amount into an electrical signal (*"photodiode" in paragraph 8)*; a select transistor for outputting to the outside accumulated electrical charge from the photoelectric conversion element following the end of exposure (*Transistor Q2 of Drawing 1, see also paragraph 8)*; one or two or more electrical charge holding circuits provided between the photoelectric conversion element and the select transistor that comprise a capacitor for temporarily holding electrical charge that has accumulated as a result of exposure from the photoelectric conversion element (*C1 of Drawing 1 which*

is between PD and transistor Q2) and a transfer transistor for controlling the transfer of the accumulated electrical charge of the photoelectric conversion element to the capacitor (*Transistor Q5 of Drawing 1, see also paragraph 12)*; and a reset transistor provided between the select transistor and the electrical charge holding circuit for discharging residual electrical charge of the capacitor prior to the start of exposure (*Transistor Q4 of Drawing 1, which is between Q2 and C1, see paragraph 8).*

Regarding Claim 15, Izawa teaches the area image sensor according to claim 2, wherein the electrical charge accumulation circuit has a constitution in which one electrode of the capacitor is connected to the output terminal of the transfer transistor and the other electrode is grounded (*drain of Q5, transfer transistor, is connected to one end of C1, capacitor, and the other end of C1 is grounded as seen in Drawing 1)*; and the input terminal of the transfer transistor is connected to the photoelectric conversion element side (*source of Q5, transfer transistor, is connected to photodiode)* and one electrode of the capacitor is connected to the reset transistor side (*one side of C1, capacitor, is connected to Q4, reset transistor, as seen in Drawing 1).*

Regarding Claim 16, Izawa teaches the area image sensor according to claim 2, with a second reset transistor for discharging residual electrical charge of the photoelectric conversion element prior to the start of exposure is connected to the input terminal of the photoelectric conversion element (*Drawing 1 shows transistor Q3, a reset transistor, connected to photodiode to discharge the PD).* However Izawa fails

to teach that in each pixel, two of the electrical charge holding circuits are connected in series between the photoelectric conversion element and the select transistor. However, one of ordinary skill in the art recognizes that connected capacitors can be connected in series for various design needs such as reducing capacitance or increasing working voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Izawa to replace the capacitor with two electrical charge holding circuits, or capacitors, in series in order to increase working voltage.

Allowable Subject Matter

1. Claims 1, 3-14, 19-23 are indicated as allowable subject matter.

2. The following is a statement of reasons for the indication of allowable subject matter: The prior art teaches an image sensor comprising similar circuitry to the instant application, and also teaches using a horizontal correction component and vertical correction component corresponding to a pixel, and uses the two components to correct the level of the photoelectric conversion signal of the corresponding pixel. The prior art teaches using the horizontal and vertical components for example by multiplying both by a suitable gain and then adding the two components. However the prior art fails to teach a pixel circuit with a reset transistor between a select transistor and electric charge holding circuit, wherein while determining a horizontal correction coefficient corresponding with a predetermined point and a vertical correction coefficient corresponding with a predetermined point, the level of the photoelectric conversion

signal of each pixel is corrected by multiplying the photoelectric conversion signal by the horizontal correction coefficient and by the vertical correction coefficient.

3. Claims 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art teaches the specifics of the pixel circuit including control lines for transfer, reset, and select which connect each pixel in a row, but fails to teach this in combination with photoelectric conversion signals of all pixels are simultaneously outputted to each row from the pixels in each row by sequentially outputting select signals to the address lines of each row in sync with an outputted plurality of horizontal and vertical synchronization signals, and with simultaneous exposure of all pixels of a time corresponding to the cycle of a vertical synchronization.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Toyoda et al. (US 7280142) teaches a solid state imaging apparatus with a defective pixel detector.

Kubo et al. (US 7106371) teaches a pixel defect detector including a calculation section for obtaining output characteristics of a subject.

Kidono et al. (US 6970193) teaches an image pickup apparatus with correction references signal generating section for generating a correction reference signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amy Hsu whose telephone number is 571-270-3012. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2622

ARH 11/10/07

LIN YE
SUPERVISORY PATENT EXAMINER